REMARKS

Claims -1-28, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-3, 7-10, 14-17, 21-24, and 28 stand rejected under 35 U.S.C. §102(b) as being anticipated by Waite (U.S. Patent No. 5,157,664). Claims 1-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by Zorian, et al. (U.S. Patent No. 7,127,647), hereinafter referred to as Zorian. Claims 1-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by McBride (U.S. Patent No. 6,829,737). Claims 4-6, 11-13, 18-20 and 25-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Waite, in view of Bartlett, et al. (U.S. Patent No. 3,761,882), hereinafter referred to as Bartlett. Applicants respectfully traverse these rejections based on the following discussion.

The present invention teaches a method and apparatus for continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device (see abstract). According to paragraph [0016] of the present application, published in U.S. Patent Application Publication No. US2005/0188289, the integrated circuit device structure 100 is designed to enable on-chip performance self-testing, self-evaluation (i.e., evaluating whether the results of self-testing are within acceptable

limits), and self-adjustment (i.e., self-adjusting parameters until the self-testing results are within acceptable limits).

A. Rejection Of Independent Claims 1, 8, 15 And 22 Based On Waite.

Waite does not teach a self-testing integrated circuit device, but rather a testing system for testing all of the individual devices on a wafer. Specifically, referring to col. 3, lines 31-68, Waite teaches in Figure 1 a test and analysis system 10 and in Figure 2 similar test and analysis system 15, which includes the same features as system 10 and further incorporates an analysis subsystem 20. The system 10 uses separate prober unit 12 that can house a wafer and that can provide the interface between the subcomponents of the tester and the individual devices that are on the wafer and that are to be tested. As discussed at col. 5, lines 55-60, the system 10 can be used to test an entire wafer containing over 300 devices in approximately 7 minutes.

More particularly, the Applicants respectfully submit that Waite does not teach or suggest the "autonomously self-monitoring and self-correcting integrated circuit device" of amended independent claims 1 and 8 or the method of "continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device" of amended independent claims 15 and 22. Specifically, Waite does not teach or suggest the following features of amended independent claim 1 or the similar features in amended independent claims 8, 15 and 22: (1) "a self-testing controller adapted to periodically perform on-chip performance self-testing of said integrated circuit device;" (2) "wherein said performance self-testing comprises application of functional test sequences to said integrated circuit device until failure"; (3) "a comparator adapted to

evaluate whether results from said self-testing are within acceptable limits;" and (5) "a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits." The cited prior art reference also does not teach or suggest the features in independent claims 8 and 22 indicating that the self-testing occurs "throughout the useful life of said integrated circuit device" and that the parameters are permanently adjusted "by altering the voltage supplied to portions of said integrated circuit device".

Specifically, the apparatus and method of the present invention include an autonomously self-monitoring and self-correcting integrated circuit device. That is, by definition, the apparatus of the present invention is an entire electronic circuit that is built onto a single piece of solid substrate (e.g., a chip) that monitors and corrects itself independently without a separate tester, etc. The Office Action indicates that Figure 1, #10 discloses this feature. The Applicant's respectfully disagree. Figure 1, #10, refers to an entire test and analysis system which uses a discrete prober unit (e.g., Electroglas, Inc. model EG 2010) to house a wafer containing many devices and to provide an interface between a tester subsystem 16 (e.g., model colt IIIA) and individual devices on the wafer. Those skilled in the art will recognize that a wafer prober is a machine used to load and unload wafers from their carriers and to align them with a probe card. The prober model cited by Waite was an automated prober developed by Electroglass in the early 1980's and used a robotic material handler for more efficient wafer handling (see http://www.electroglas.com/company/history.shtml). Thus, the testing system 10 is not an

autonomously self-monitoring and self-correcting integrated circuit device, but rather a system to test wafers.

The Office Action further provides that Waite discloses "a self-testing controller (Figure 2#22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device." The Applicant's respectfully disagree. Per col. 3, lines 60-68, the analysis subsystem 20 of system 15 generates repair and analysis information which can be transferred to a microcomputer (item 22 of Figure 2) via interfacing hardware. The cited portion of Waite (i.e., col. 5, lines 14-21) provides "One feature of the invention is recognition that the speed of the test and analysis process is severely limited by the prior art serial test and analysis sequence which has utilized a single microprocessor to perform control functions as well as computation tasks related to scanning the fail memory and determining which lines should be replaced." Thus, Figure 2 incorporates the analysis subsystem 20 to allow the tester subsystem 16 to operate on one device and the analysis subsystem 20 to analyze data formerly collected by the tester subsystem 16 on another device (see col. 5, lines 45-50). No where in Waite is it taught or disclosed that the microcomputer 22 is a component of a self-monitoring and self-correcting integrated circuit, which also includes the product to be tested. Furthermore, no where in Waite does it teach or suggest that the microprocessor 22 is adapted to perform performance testing, much less to periodically perform on-chip performance self-testing. The microprocessor 22 of Waite is not a self-testing controller, but rather one place that data developed by the analysis subsystem 20 can be sent after wafer testing.

The Office Action provides that Waite discloses "a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 1 #42)." The Applicants respectfully disagree. Per col. 5, lines 52-59, item 42 of Figure 1 refers to comparator circuitry in the tester subsystem 16 that looks at differences between the read data from the device under test to expected data and makes a pass-fail decision. However, no where in Waite is it taught or disclosed that the data compare circuitry 42 is a component of a self-monitoring and self-correcting integrated circuit, which also includes the product to be tested.

The Office Action provides that Waite discloses "a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 2, lines 60-67)." The Applicants respectfully disagree. Col. 2, lines 60-67, of Waite provides "The tester subsystem is operable in conjunction with a probe unit to write a test pattern to the memory device under test and read binary values store in the memory device. Comparator circuitry is coupled to the tester subsystem to provide information identifying defective cells in the memory device based on differences between the test pattern and binary values read from the memory device. A fail memory stores the output of the comparator circuitry." No where in Waite does it teach or disclose adjusting the integrated circuit parameters until the results are within acceptable limits. Rather defective cells are identified in the comparator circuitry and a fail memory stores the output of the comparator circuitry. Col. 5, lines 38-50, provides that analysis system 20 can develop and output a repair scheme to a repair

system for subsequent implementation. However, Waite does not disclose "a processor" that is a component a self-monitoring and self-correcting integrated circuit, which also includes the product to be tested. Nor does Waite teach or suggest a processor that is "adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits." Rather per col. 5, lines 0-12, the analysis system 20 of Waite can develop a repair scheme and *output* that repair scheme to a repair system for subsequent implementation.

The additional features in amended independent claims 8 and 22 of "throughout the useful life of said integrated circuit device" and "by altering the voltage supplied to portions of said integrated circuit device" are also not taught by Waite. Since the system of Waite involves wafer testing, it necessarily does not disclose the ability to test the circuit "throughout the useful life of said integrated circuit device." Additionally, the Office Action acknowledges that the feature of self-adjusting the integrated circuit parameters by altering the voltage supplied to portions of the integrated circuit device is not taught by Waite and, therefore, cites col. 19, lines 4-15 of Bartlett. The Applicants respectfully disagree.

The cited portion of Bartlett provides "Thus, in case of error in writing or in a situation where it is desired to expand a previous instruction repertoire, it is only necessary to open circuit the remaining diode-fuse combinations in any memory location. This will result in an instruction of 000, interpreted as an AND instruction, coupled with the address 0. Location 0 is permanently wired to the power source so that this operation corresponds to an AND 1. Those skilled in the art will readily understand that ANDing

anything with a 1 will result in what had previously been present and therefore this is another type of "no instruction" operation. No where in Bartlett does it teach or suggest permanently self-adjusting integrated circuit parameters by altering the voltage supplied to portions of the integrated circuit device until the results from the self-testing are within the acceptable limits.

Therefore, amended independent claims 1, 8, 15 and 22 are patentable over Waite. Further, dependent claims 2-7, 9-14, 16-21 and 23-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Rejection Of Independent Claims 1, 8, 15 And 22 Based On Zorian.

The Applicants also respectfully submit that Zorian does not teach or suggest the "autonomously self-monitoring and self-correcting integrated circuit device" of amended independent claims 1 and 8 or the method of "continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device" of amended independent claims 15 and 22. Specifically, Zorian does not teach or suggest the following features of amended independent claim 1 or the similar features in amended independent claims 8, 15 and 22: (1) "a self-testing controller adapted to periodically perform on-chip performance self-testing of said integrated circuit device;" (2) "wherein said performance self-testing comprises application of functional test sequences to said

integrated circuit device until failure;" (3) "a comparator adapted to evaluate whether results from said self-testing are within acceptable limits;" and (4) "a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits." The cited prior art reference also does not teach or suggest the feature in independent claims 8 and 22 indicating that the parameters are permanently adjusted "by altering the voltage supplied to portions of said integrated circuit device".

Per the Abstract Zorian teaches a method and system that determines allocation of one or more redundant components to repair one or more defects detect in the memory while fault testing the memory. The Office Action provides that Zorian discloses "A self-testing controller (Figure 3 "BIST") adapted to periodically perform performance self-testing on said integrated circuit device (column 5 lines 5-25)". The Office Action further provides that Zorian discloses "a functional testing unit (col. 3, lines 20-25)" and "apply functional test sequences (col. 6, lines 20-25) to said integrated circuit device until failure (Figure 1#34). The Applicants respectfully disagree.

The self-testing referred to in Zorian is fault testing, as opposed to the performance testing by applying functional test sequences. Specifically, those skilled in the art will recognize that performance testing generally refers to testing to determine whether the system/circuit is in compliance with specified performance requirements. Contrarily, the cited portion of Zorian discloses a BIST engine for performing tests designed *to detect defects in the memories* and a BISD engine for determining the location of those defects. Col. 6, lines 20-25 refer to an intelligent wrapper disclosed as

an extension of the processor in Zorian. This wrapper is used in conjunction with the processor to perform testing and repair as well as to allow normal memory functioning. The wrapper includes functions such as address counters, registers, comparators and is close to the memory core to allow testing of those functions (i.e., of address counters, registers, etc.). No where in Zorian does it teach or disclose that the self-testing controller adapted to periodically perform on-chip performance self-testing of said integrated circuit device, much less that this performance self-testing comprises application of functional test sequences to the integrated circuit device until failure.

The Office Action further provides that Zorian discloses "a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (column 6, lines 5-35)." The Applicants respectfully disagree. Col. 6, lines 5-12, refers to the fact that the memories in Zorian may be the same or different sizes and that a single fuse box can serve all of the memories. Col. 6, lines 14-32, refers to the intelligent wrapper, discussed above, which contains various functions including data comparators. However, the purpose of such data comparators is not disclosed. Col. 6, lines 33-35, refers only to a block diagram of a memory. No where in Zorian does it disclose that the comparator is adapted to evaluate whether results from self-testing are within acceptable limits.

The Office Action further provides that Zorian discloses "a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 7, lines 20-45)." The Applicants respectfully disagree. The cited portion of Zorian describes a block diagram of a redundancy engine

having a plurality of registers. After detecting a defective memory cell, the BIST engine sends the address of the defective cell to the redundancy engine for processing. Status bit registers indicate whether a redundant row is available or unavailable as a substituting row for a faulty row. No where in Zorian does it teach or disclose a processor adapted to adjust parameters of the integrated circuit device until the results from the self-testing are within the acceptable limits.

The additional feature in amended independent claims 8 and 22 of self-adjusting the integrated circuit device parameters "by altering the voltage supplied to portions of said integrated circuit device" is also not taught or suggested by Zorian. The Office Action cites Zorian as disclosing "wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit by using voltage regulators (column 4, lines 50-65)." The Applicants respectfully disagree. Col. 4, lines 50-54, discusses the benefits of the processor 206 of Zorian (i.e., reduction of external test stages from 4 to 1). Col. 4, lines 55-60, indicates that the system of Zorian supports both at factory and in the field testing and repair. Col. 4, lines 60-65, indicates that during at factor testing the wafer can be subjected to stringent conditions that help insure high memory instance and system on chip reliability during extended voltage, temperature and frequency conditions. Nothing in the cited portions of Zorian teaches or discloses that, after self-testing, the voltage supplied to portions of the integrated circuit device is altered in order to permanently adjust the integrated circuit parameters until the self-testing results are within acceptable limits.

Therefore, amended independent claims 1, 8, 15 and 22 are patentable over Zorian. Further, dependent claims 2-7, 9-14, 16-21 and 23-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

C. Rejection Of Independent Claims 1, 8, 15 and 22 Based on McBride.

The Applicants further respectfully submit that McBride does not teach or suggest the "autonomously self-monitoring and self-correcting integrated circuit device" of amended independent claims 1 and 8 or the method of "continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device" of amended independent claims 15 and 22. Specifically, McBride does not teach or suggest the following features of amended independent claim 1 or the similar features in amended independent claims 8, 15 and 22: (1) "wherein said performance self-testing comprises application of functional test sequences until failure"; and (2) "a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits." The cited prior art reference also does not teach or suggest the feature in independent claims 8 and 22 indicating that the parameters are permanently adjusted "by altering the voltage supplied to portions of said integrated circuit device".

Per the Abstract, McBride teaches a method and system for testing a semiconductor device and for storing the testing results on that tested device. The Office Action cites McBride as disclosing "a functional testing unit (column 6, lines 20-25)" and "wherein said functional testing unit is adapted to apply functional test sequences (column 6, lines 20-25) to said integrated circuit device until failure (Figure 1 #34)". The Applicants respectfully disagree. Figure 1 does not appear to contain a #34. Col. 6, lines 20-25, provides "The relationship between the test result and the setting of non-volatile memory element 14 will generally follow a predetermined rule. In the simplest case, the rule will be that for a particular test result, the latch will always be set to a particular value. For example, comparator circuit 11 may be configured to set test latch 12 to a logical high value if the value on output line 102 matches the expected value, i.e., the test step is failed." Thus, the cited portions of McBride do not disclose the application of functional test sequences, just testing in general. Further McBride does not disclose the application of functional test sequences until failure, but rather an example of how to set the non-volatile memory if a particular testing result, such as failure, is output.

The Office Action further cites McBride as disclosing "a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 7, lines 20-45)." The Applicants respectfully disagree. Col. 7, lines 20-45, refers to an additional embodiment of McBride in which the test circuitry is divided into subsections, each with a plurality of nonvolatile memory elements for storing the testing results from a particular subsection of the device. No

where in the McBride does it teach or suggest "a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits." Rather McBride only teaches storing the results.

The additional feature in amended independent claims 8 and 22 of self-adjusting the integrated circuit device parameters "by altering the voltage supplied to portions of said integrated circuit device" is also not taught or suggested by McBride. The Office Action cites McBride as disclosing "wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit by using voltage regulators (column 4, lines 50-65)." As discussed above, McBride does not teach self-adjusting the integrated circuit device parameters until the results for the self-testing are within the acceptable limits. Col. 4, lines 50-55, of McBride indicates that the nonvolatile memory elements that store testing results may be memory elements already on the integrated circuit device. Col. 4, lines 55-65, of McBride indicates that send/receive locations (included in the test circuitry) may be memory locations if the device under test is a memory device or input/outputs to an integrated circuit device if the device under test is some other type of device. The send/receive locations are employed in normal integrated circuit functioning and other components of the test circuitry are included for testing purposes only. Nothing in McBride teaches or discloses that, after self-testing, the voltage supplied to portions of the integrated circuit device is altered in order to permanently adjust the integrated circuit parameters until the self-testing results are within acceptable limits.

Therefore, amended independent claims 1, 8, 15 and 22 are patentable over McBride. Further, dependent claims 2-7, 9-14, 16-21 and 23-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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